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CLAIMS

The invention claimed is:

1. A method of forming conductively-doped regions relative to a pair of adjacent transistor gates, comprising:

partially forming a pair of adjacent transistor gates over a semiconductor substrate, the partially-formed transistor gates having a layer of conductive material extending between them;

forming at least one conductively-doped region between the partially-formed adjacent transistor gates; and

after forming the at least one conductively-doped region, removing the layer of conductive material from between the adjacent transistor gates.

2. The method of claim 1 wherein at least one conductively-doped region includes a pair of regions extending to under the partially-formed adjacent transistor gates.

3. The method of claim 1 wherein the conductive material consists of conductively doped silicon.

4. The method of claim 1 wherein the conductive material consists of conductively doped silicon and has a thickness of from about 100Å to about 400Å.

5. The method of claim 1 wherein the at least one conductively-doped region comprises an L_{DD} region.

6. The method of claim 1 wherein the at least one conductively-doped region includes a pair of pocket implant regions, and further comprising forming a heavily-doped source/drain region extending between the pocket implant regions and shared by the adjacent transistor gates.

7. The method of claim 1 wherein the at least one conductively-doped region includes a pair of pocket implant regions and an L_{DD} region.

8. The method of claim 1 further comprising incorporating the adjacent transistor gates into a pair of adjacent DRAM cells, the adjacent cells sharing a bitline connection.

9. The method of claim 1 wherein the partially formed transistor gates have sidewall edges, and further comprising forming electrically insulative sidewall spacers along the sidewall edges of the partially formed transistor gates.

10. A method of forming angled implants relative to a pair of adjacent transistor gates, comprising:

forming a gate stack over a substrate, the gate stack comprising a layer of electrically conductive material;

etching only partially through the layer of electrically conductive material to leave an unetched remaining portion of the electrically conductive material and to partially form a pair of adjacent transistor gates from the gate stack;

implanting at least one dopant at an angle other than 0° relative to vertical to form pocket implant regions under the partially formed adjacent transistor gates; and

after the implanting, etching through the remaining portion of the electrically conductive material and completing formation of the pair of adjacent transistor gates.

11. The method of claim 10 wherein the partially formed transistor gates have sidewall edges, and further comprising forming electrically insulative sidewall spacers along the sidewall edges of partially formed transistor gates.

12. The method of claim 10 further comprising forming a heavily-doped source/drain region shared by the adjacent transistor gates; the forming the heavily-doped source/drain region occurring before the formation of the pocket regions.

13. The method of claim 10 further comprising forming a heavily-doped source/drain region shared by the adjacent transistor gates; the forming the heavily-doped source/drain region occurring after the formation of the pocket regions.

14. The method of claim 13 wherein the forming the heavily-doped source/drain region occurs prior to the etching through the remaining portion of the electrically conductive material.

15. The method of claim 13 wherein the forming the heavily-doped source/drain region occurs after the etching through the remaining portion of the electrically conductive material.

16. The method of claim 10 wherein the layer of electrically conductive material comprises conductively-doped silicon.

17. The method of claim 10 wherein the layer of electrically conductive material consists of conductively-doped silicon.

18. The method of claim 17 wherein the layer of electrically conductive material is a first layer of conductive material; and wherein the gate stack comprises:

a pad oxide layer between the first layer of conductive material and the substrate;

at least one more layer of conductive material over the first layer of conductive material; and

an insulative layer over the at least one more layer of conductive material.

19. The method of claim 18 wherein the at least one more layer of electrically conductive material comprises a layer of tungsten over a layer of tungsten nitride.

20. The method of claim 18 wherein the insulative layer comprises silicon nitride.

21. A method of forming angled implants relative to a pair of adjacent transistor gates, comprising:

forming a gate stack over a substrate, the gate stack comprising a first layer;

etching only partially through the first layer to leave an unetched remaining portion of the first layer and to partially form a pair of adjacent transistor gates from the gate stack, the partially formed transistor gates have sidewall edges;

forming a second layer along the sidewall edges of the partially formed pair of adjacent transistor gates;

after forming the second layer, implanting at least one dopant at an angle other than 0° relative to vertical to form pocket implant regions under the partially formed adjacent transistor gates; and

after the implanting, etching through the remaining portion of the first layer and completing formation of the pair of adjacent transistor gates.

22. The method of claim 21 further comprising anisotropically etching the second layer prior to the etching of the remaining portion of the first layer.

23. The method of claim 21 wherein the first layer is an electrically conductive material.

24. The method of claim 21 wherein the first layer consists of conductively doped silicon.

25. The method of claim 21 wherein the second layer is an electrically insulative material.

26. The method of claim 21 wherein the second layer consists of silicon nitride.

27. The method of claim 21 wherein the first layer is an electrically conductive material and the second layer is an electrically insulative material.

28. The method of claim 21 wherein the first layer consists of conductively doped silicon and the second layer consists of silicon nitride.

29. A method of forming a DRAM assembly, comprising:

forming a gate stack over a substrate, the gate stack comprising a layer of electrically conductive material;

etching only partially through the layer of electrically conductive material to leave an unetched remaining portion of the electrically conductive material and to partially form a pair of adjacent transistor gates from the gate stack; one of the adjacent transistor gates ultimately being incorporated into a first DRAM cell and the other of the adjacent transistor gates ultimately being incorporated into a second DRAM cell;

forming pocket implant regions under the partially formed transistor gates;

after the forming the pocket implant regions, etching through the remaining portion of the electrically conductive material, and completing formation of the pair of adjacent transistor gates;

forming a heavily doped source/drain region shared by the adjacent transistor gates;

forming first and second data storage devices for the first and second DRAM cells, respectively; and

forming a bitline contact in electrical with the source/drain region.

30. The method of claim 29 wherein the data storage devices are capacitors.

31. The method of claim 29 wherein the forming the heavily-doped source/drain region occurs before the formation of the pocket regions.

32. The method of claim 29 wherein the forming the heavily-doped source/drain region occurs after the formation of the pocket regions.

33. The method of claim 32 wherein the forming the heavily-doped source/drain region occurs prior to the etching through the remaining portion of the electrically conductive material.

34. The method of claim 32 wherein the forming the heavily-doped source/drain region occurs after the etching through the remaining portion of the electrically conductive material.

35. The method of claim 29 wherein the layer of electrically conductive material consists of conductively-doped silicon.

36. The method of claim 35 wherein the layer of electrically conductive material is a first layer of conductive material; and wherein the gate stack comprises:

a pad oxide layer between the first layer of conductive material and the substrate;

at least one more layer of conductive material over the first layer of conductive material; and

an insulative layer over the at least one more layer of conductive material.

37. The method of claim 36 wherein the at least one more layer of electrically conductive material comprises a layer of tungsten over a layer of tungsten nitride.

38. The method of claim 36 wherein the insulative layer comprises silicon nitride.

39. A method of forming a pair of adjacent memory cells sharing a common bitline, comprising:

forming a gate stack over a substrate, the gate stack comprising a layer of electrically conductive material;

etching only partially through the layer of electrically conductive material to leave an unetched remaining portion of the electrically conductive material and to partially form a pair of adjacent transistor gates from the gate stack; one of the adjacent transistor gates ultimately being incorporated into a first transistor and the other of the adjacent transistor gates ultimately being incorporated into a second transistor;

defining three source/drain region locations relative to the partially formed transistor gates, a first of the source/drain region locations being associated with only the first transistor; a second of the source/drain region locations being shared by the first and second transistors, and a third of the source/drain region locations being associated with only the second transistor;

forming a mask over the first and third source/drain region locations;

while the mask is over the first and third source/drain region locations, implanting at least one dopant at an angle other than 0° relative to vertical to form pocket implant regions under the partially formed transistor gates;

after the implanting, removing the mask, etching through the remaining portion of the electrically conductive material, and completing formation of the pair of adjacent transistor gates;

forming first, second and third heavily doped source/drain regions

at the first, second and third source/drain region locations, respectively;

forming first and second data storage devices in electrical connection with the first and third source/drain regions, respectively; and

forming a bitline contact in electrical with the second source/drain region.

40. The method of claim 39 further comprising, while the mask is over the first and third source/drain region locations, implanting at least one dopant to form an L_{DD} region between the partially formed transistor gates.

41. The method of claim 39 wherein the data storage devices are capacitors.

42. The method of claim 39 wherein the forming the heavily-doped source/drain regions occurs before the formation of the pocket regions.

43. The method of claim 39 wherein the forming the heavily-doped source/drain regions occurs after the formation of the pocket regions.

44. The method of claim 43 wherein the forming the heavily-doped source/drain regions occurs prior to the etching through the remaining portion of the electrically conductive material.

45. The method of claim 43 wherein the forming the heavily-doped source/drain regions occurs after the etching through the remaining portion of the electrically conductive material.

46. The method of claim 39 wherein the layer of electrically conductive material comprises conductively-doped silicon.

47. The method of claim 39 wherein the layer of electrically conductive material consists of conductively-doped silicon.

48. The method of claim 47 wherein the layer of electrically conductive material is a first layer of conductive material; and wherein the gate stack comprises:

a pad oxide layer between the first layer of conductive material and the substrate;

at least one more layer of conductive material over the first layer of conductive material; and

an insulative layer over the at least one more layer of conductive material.

49. The method of claim 48 wherein the at least one more layer of electrically conductive material comprises a layer of tungsten over a layer of tungsten nitride.

50. The method of claim 48 wherein the insulative layer comprises silicon nitride.

51. A method of forming an electronic system, comprising:

forming a gate stack over a substrate, the gate stack comprising a layer of electrically conductive material;

etching only partially through the layer of electrically conductive material to leave an unetched remaining portion of the electrically conductive material and partially forming transistor gates from the gate stack; at least some of the partially formed transistor gates being paired adjacent transistor gates;

forming pocket implant regions under at least some of the partially formed paired adjacent transistor gates;

after the forming the pocket implants, etching through the remaining portion of the electrically conductive material, and completing formation of the transistor gates;

forming source/drain regions proximate the transistor gates, some of the source/drain regions being shared by paired adjacent transistor gates;

forming data storage devices in electrical connection with at least some of the source/drain regions;

forming bitline contacts in electrical with at least some of the shared source/drain regions; the data storage devices, paired adjacent transistors and bitline contacts being incorporated into an array of memory cells;

forming addressing circuitry coupled to the array of memory cells for accessing individual memory cells in the array of memory cells; and

forming a read circuit coupled to the array of memory cells for reading data from memory cells in the array of memory cells.

52. The method of claim 51 wherein the memory cells are incorporated into devices selected from the group consisting of SDRAM, DDR SDRAM, SLDRAM, Direct RDRAM, SRAM, VRAM, EEPROM, and Flash memories.

53. The method of claim 51 wherein the data storage devices are capacitors.

54. The method of claim 51 wherein the forming the heavily-doped source/drain regions occurs before the formation of the pocket regions.

55. The method of claim 51 wherein the forming the heavily-doped source/drain regions occurs after the formation of the pocket regions.

56. The method of claim 55 wherein the forming the heavily-doped source/drain regions occurs prior to the etching through the remaining portion of the electrically conductive material.

57. The method of claim 55 wherein the forming the heavily-doped source/drain regions occurs after the etching through the remaining portion of the electrically conductive material.

58. The method of claim 51 wherein the layer of electrically conductive material consists of conductively-doped silicon.

59. The method of claim 58 wherein the layer of electrically conductive material is a first layer of conductive material; and wherein the gate stack comprises:

a pad oxide layer between the first layer of conductive material and the substrate;

at least one more layer of conductive material over the first layer of conductive material; and

an insulative layer over the at least one more layer of conductive material.

60. The method of claim 59 wherein the at least one more layer of electrically conductive material comprises a layer of tungsten over a layer of tungsten nitride.

61. The method of claim 59 wherein the insulative layer comprises silicon nitride.